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				Art Unit	TBD
				Examiner Name	TBD
Sheet	1	of	2	Attorney Docket Number	2004 P 50201 US

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Substitute for form 1449B/PTO		Complete If Known	
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		First Named Inventor	Li
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		Examiner Name	TBD
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Sheet	2	of	2

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
SK	2	KING, A.C., <i>et al.</i> , "Surface Proximity Effect on End-of-Range Damage of Low Energy Ge ⁺ Implantation," Ultra Shallow Junctions 2003, Seventh International Workshop on: Fabrication, Characterization, and Modeling of Ultra-Shallow Doping Profiles in Semiconductors, April 27-May 1, 2003, pp. 447-450, Santa Cruz, CA, USA.	
SK	3	STRAUBE, U.N., <i>et al.</i> , "Adverse Effect of Ge ⁺ Implantation for Fabrication of SiGe PMOS," Electronics Letters, December 6, 2001, pp. 1549-1550, Vol. 37, No. 25.	
SK	4	SELVAKUMAR, C.R., <i>et al.</i> , "SiGe-Channel n-MOSFET by Germanium Implantation," IEEE Electron Device Letters, August, 1991, pp. 444-446, Vol. 12, No. 8, IEEE, New York, NY, USA.	
	5	JIANG, H., <i>et al.</i> , "Electrical Properties of GeSi Surface- and Buried- Channel p-MOSFET's Fabricated by Ge Implantation," IEEE Transactions on Electron Devices, January, 1996, pp. 97-103, Vol. 43, No. 1, IEEE, New York, NY, USA.	
	6	JOHN, S., <i>et al.</i> , "Strained Si n-Channel Metal-Oxide-Semiconductor Transistor on Relaxed Si _{1-x} Ge _x Formed by Ion Implantation of Ge," Applied Physics Letters, April 5, 1999, pp. 2076-2078, Vol. 74, No. 14, American Institute of Physics, College Park, MD, USA.	
	7	LIU, K.C., <i>et al.</i> , "A Deep Submicron Si _{1-x} Ge _x /Si Vertical PMOSFET Fabricated by Ge Ion Implantation," IEEE Electron Device Letters, January, 1998, pp. 13-15, Vol. 19, No. 1, IEEE, New York, NY, USA.	
	8	NGUYEN, N.V., <i>et al.</i> , "Characterization of the Interface Between Ge ⁺ -Implanted Crystalline Silicon and its Thermally Grown Oxide by Spectroscopic Ellipsometry," Journal of Applied Physics, January 15, 1990, pp. 599-603, Vol. 67, No. 2, American Institute of Physics, College Park, MD, USA.	
	9	HÖCK, G., <i>et al.</i> , "High Hole Mobility in Si _{0.17} Ge _{0.83} Channel Metal-Oxide-Semiconductor Field-Effect Transistors Grown by Plasma-Enhanced Chemical Vapor Deposition," Applied Physics Letters, June 26, 2000, pp. 3920-3922, Vol. 76, No. 26, American Institute of Physics, College Park, MD, USA.	
	10	SHANG, H., <i>et al.</i> , "High Mobility p-Channel Germanium MOSFETs with a Thin Ge Oxyntride Gate Dielectric," 2002, 0-7803-7463-X/02, IEEE, New York, NY, USA.	
	11	LEE, M.L., <i>et al.</i> , "Strained Ge Channel p-Type Metal-Oxide-Semiconductor Field-Effect Transistors Grown on Si _{1-x} GySi Virtual Substrates," Applied Physics Letters, November 12, 2001, pp. 3344-3346, Vol. 79, No. 20, American Institute of Physics, College Park, MD, USA.	
	12	CHUI, C.O., <i>et al.</i> , "Germanium MOS Capacitors Incorporating Ultrathin High-x Gate Dielectric," IEEE Electron Device Letters, August, 2002, pp. 473-475, Vol. 23, No. 8, IEEE, New York, NY, USA.	
	13	CHUI, C.O., <i>et al.</i> , "A Sub-400°C Germanium MOSFET Technology with High-x Dielectric and Metal Gate," 2002, 0-7803-7463-X/02, IEEE, New York, NY, USA.	
	14	ZOLLNER, S., <i>et al.</i> , "Optical Constants and Ellipsometric Thickness Determination of Strained Si _{1-x} Ge _x :C Layers on Si (100) and Related Heterostructures," Journal of Applied Physics, October 1, 2000, pp. 4102-4108, Vol. 88, No. 7, American Institute of Physics, College Park, MD, USA.	
	15	LEGOUES, F.K., <i>et al.</i> , "Oxidation Studies of SiGe," Journal of Applied Physics, February 15, 1989, pp. 1724-1728, Vol. 65, No. 4, American Institute of Physics, College Park, MD, USA.	
	16	PLUMMER, et al., Silicon VLSE Technology, Fundamentals, Practice and Modeling, 2000, p. 453, Prentice Hall, Upper Saddle River, NJ.	
	17	"Front End Processes," International Technology Roadmap for Semiconductor (ITRS), 2002 Update, pp. 45-62, http://member.itrs.net/ .	
SK	18	"Front End Processes," International Technology Roadmap for Semiconductor (ITRS), 2003 Edition, pp. 23-25, http://member.itrs.net/ .	

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